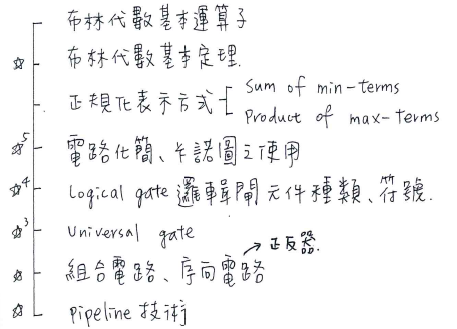
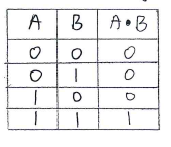
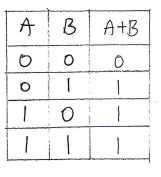
CH 6 數位邏輯



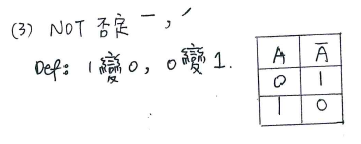
1. 布林代數基本運算
   * AND (•)
     + Input 皆為1的時候為1，否則為0



* + OR(+)
    - Input 皆為0的時候為0，否則為1(有1個為1就1)

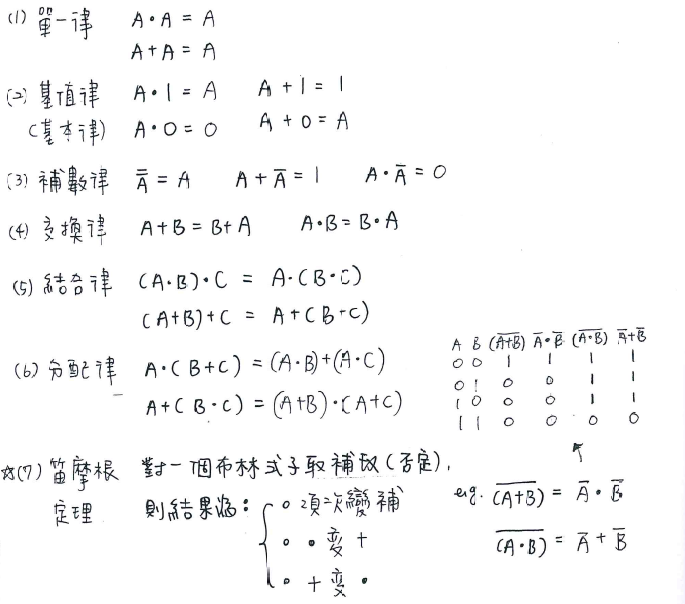


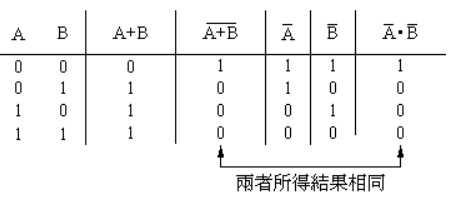
* + NOT

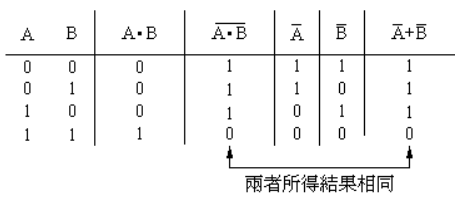


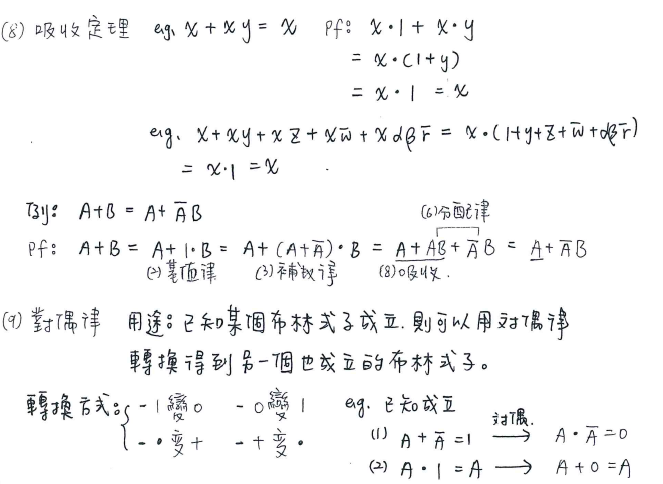


1. 布林代數基本定理(9個)

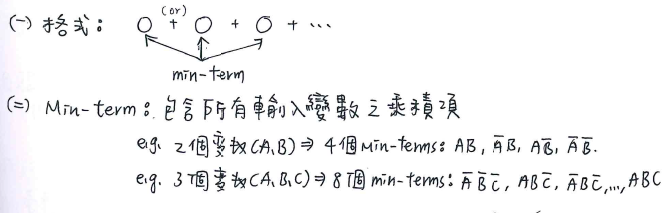




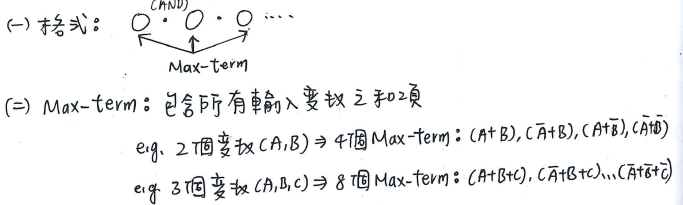


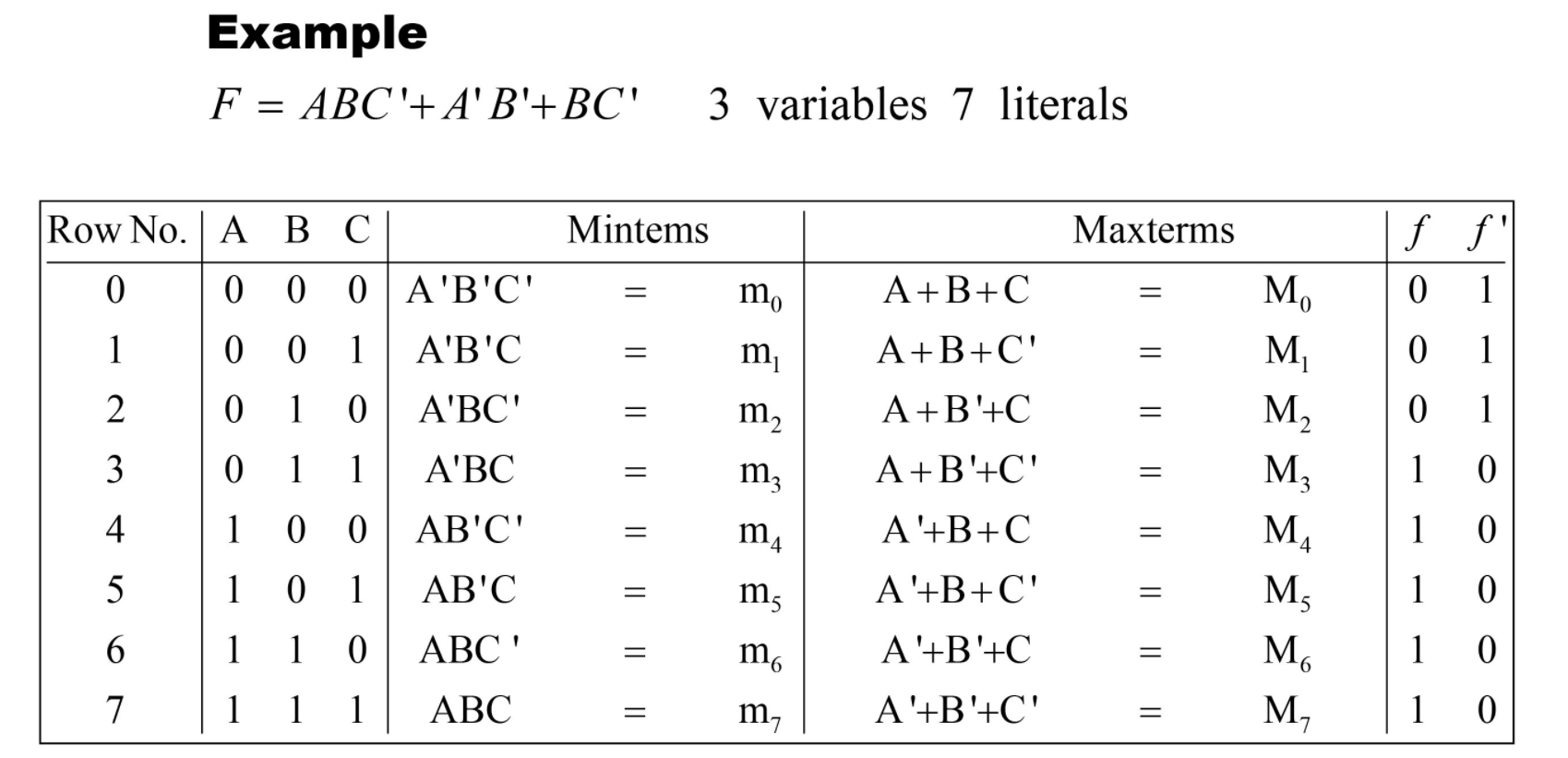


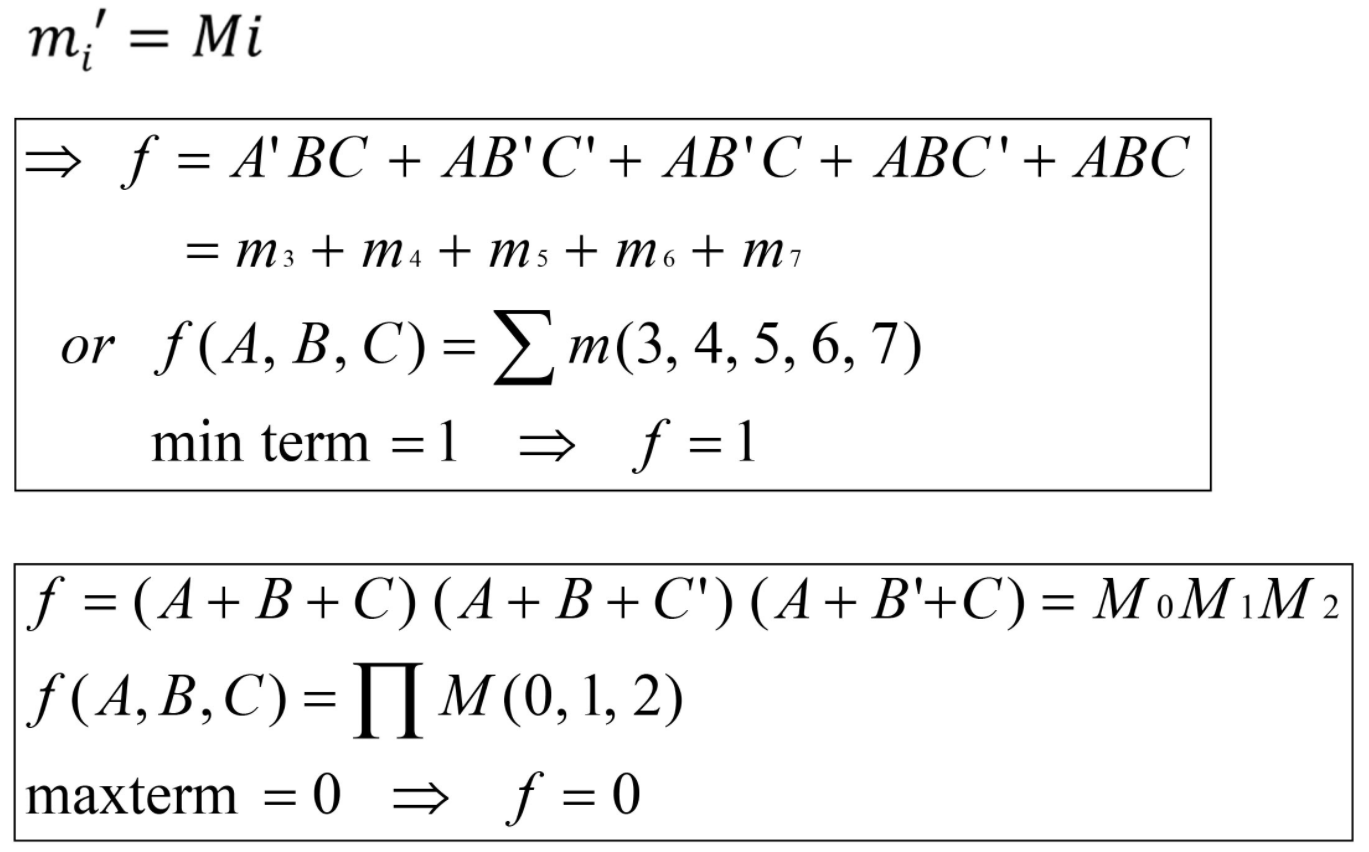
1. 正規化表示法
   * 「最小項的和」(sum of minterms)
     + 將最小項以「OR」運算子結合，也就是用「＋」運算子結合，便是「最小項的和」
     + N個變數，個組合



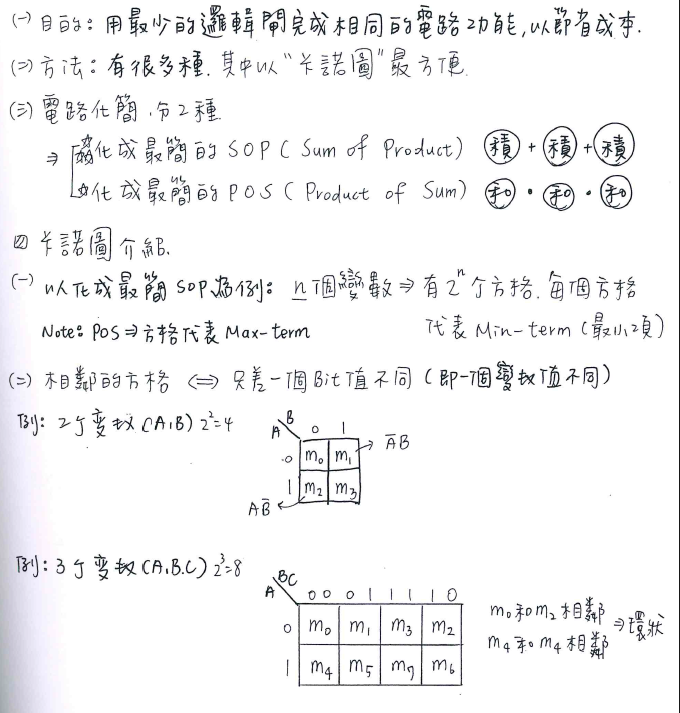
* + 「最大項的積」(product of maxterms)
    - 將最大項以「AND」運算子結合，也就是用「‧」運算子結合，便是「最大項的積」



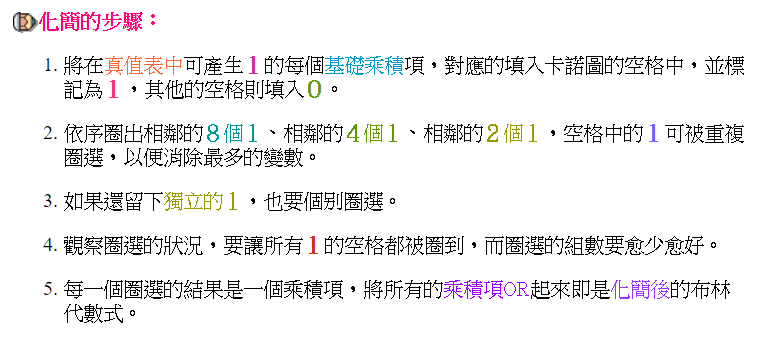


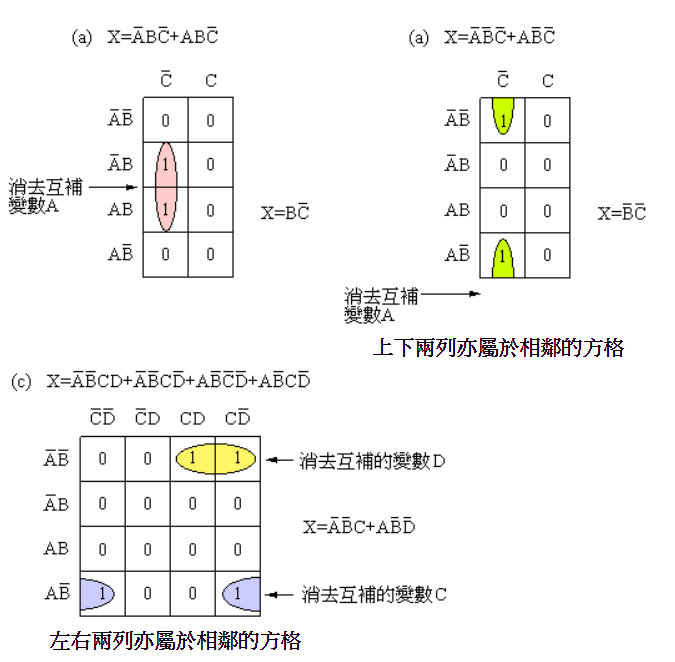


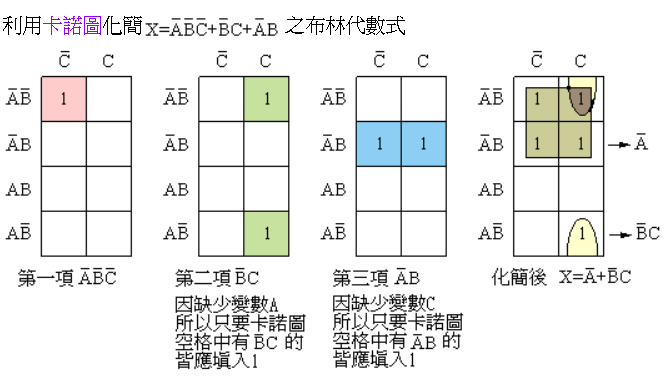
1. 電路化簡



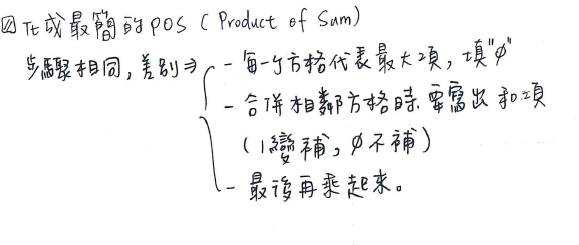
* + SOP(卡諾圖)

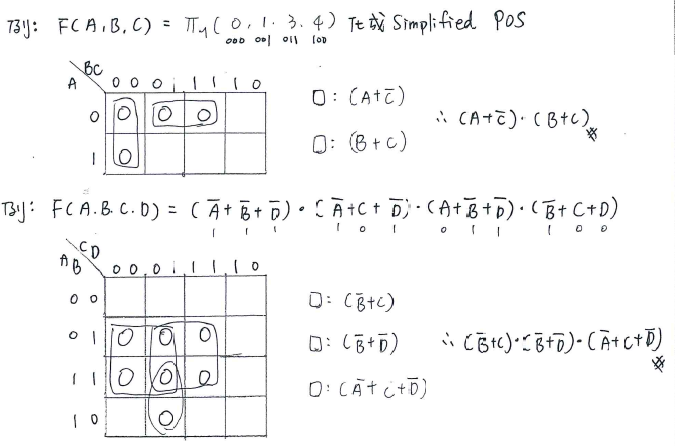




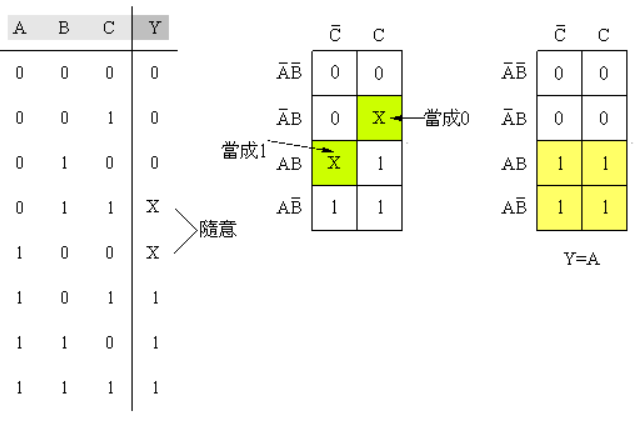


* + POS

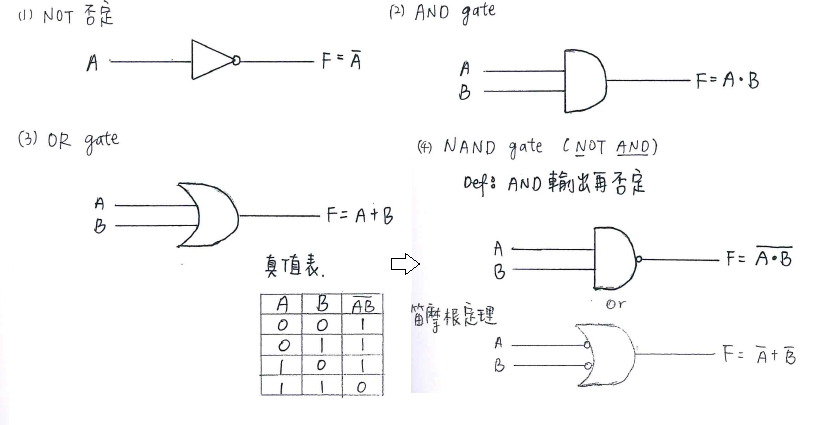


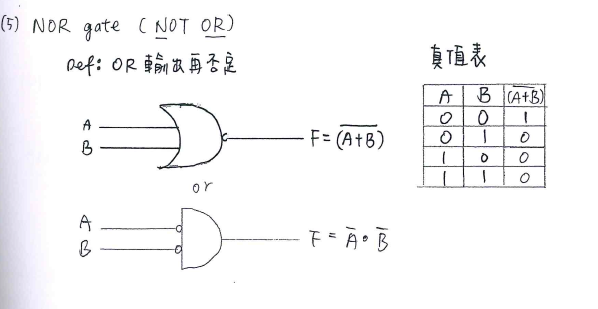


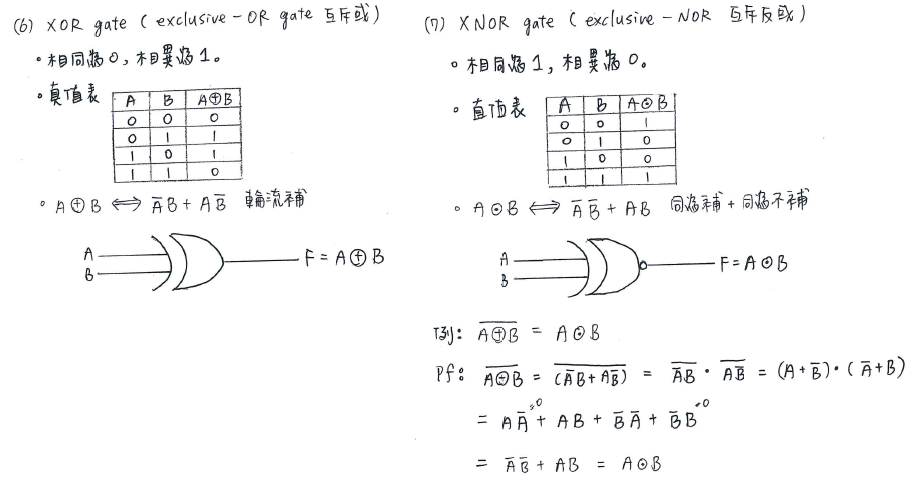
* + 隨意條件(Don’t care condition)
    - 並非所有的輸入狀況皆會發生，其對輸出不重要

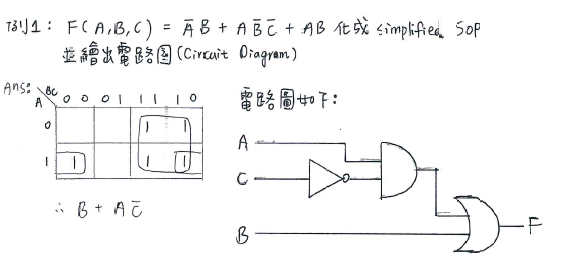


1. 邏輯閘(Logic Gate)

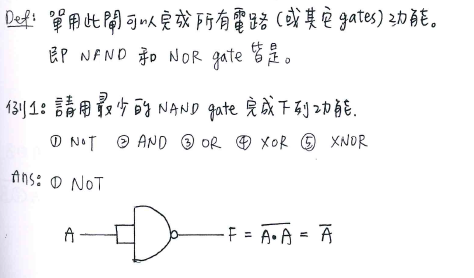




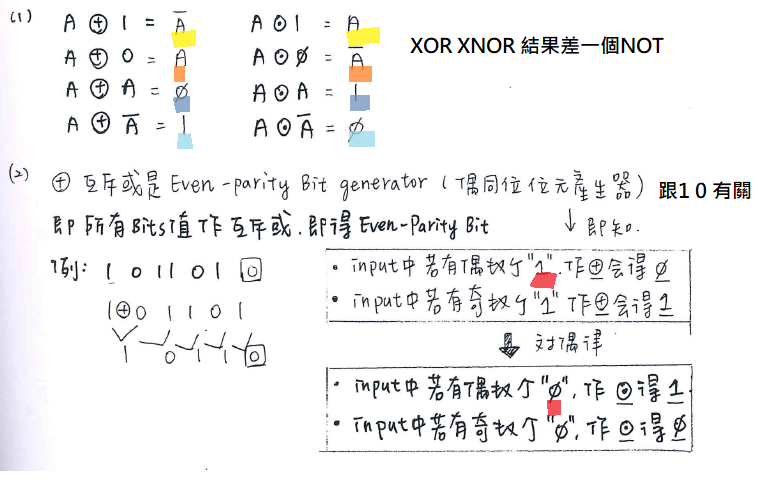




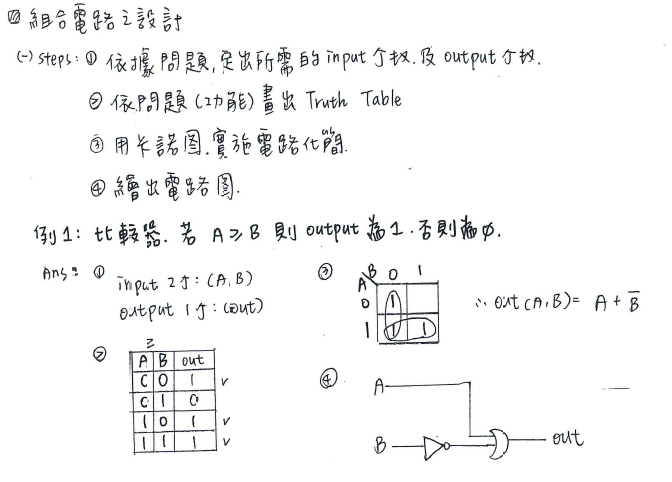
1. Universal Gate C Complete Gate 萬用閘/完整閘

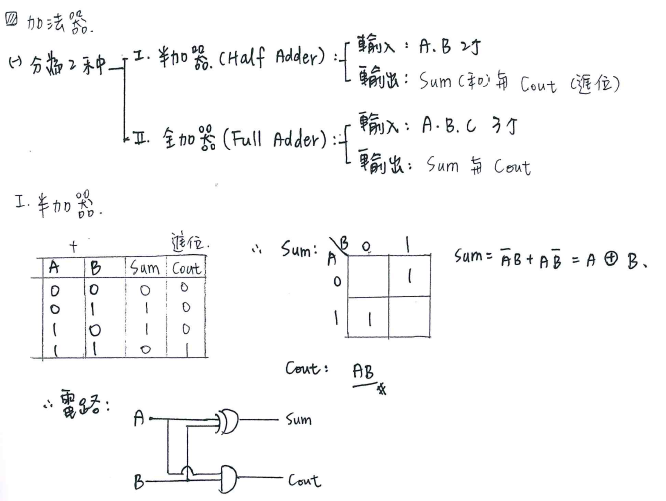


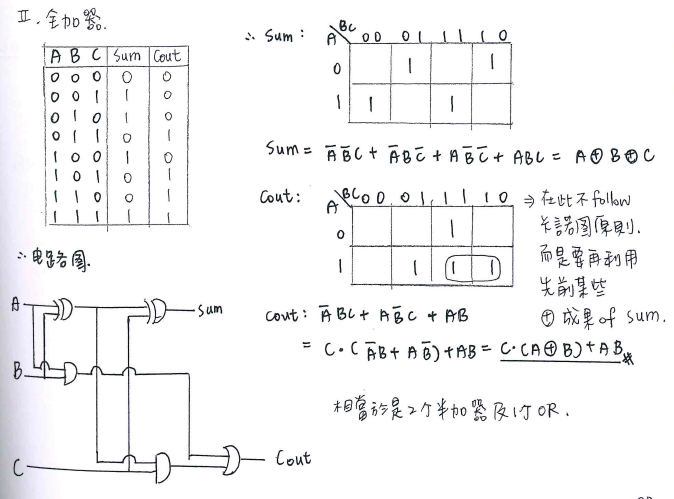
1. XOR與XNOR特性探討

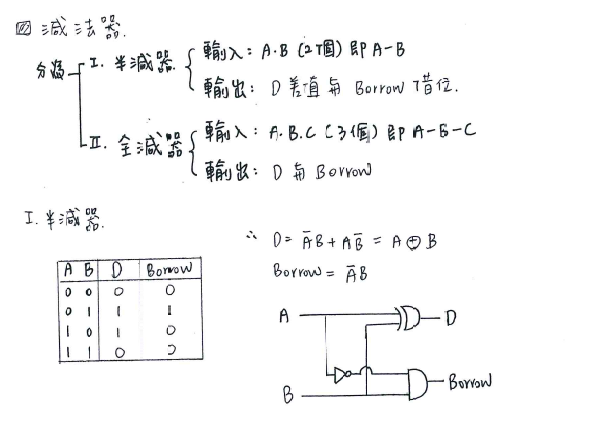


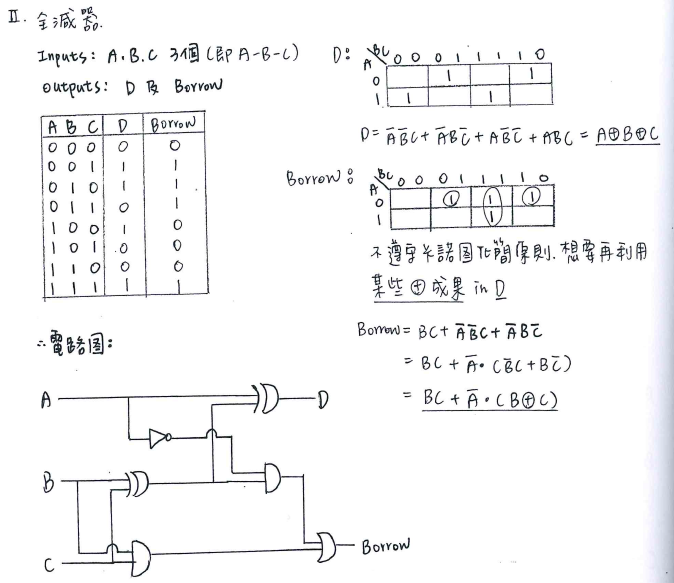
1. 電路種類
   * 組合電路(Combinational Circuit)



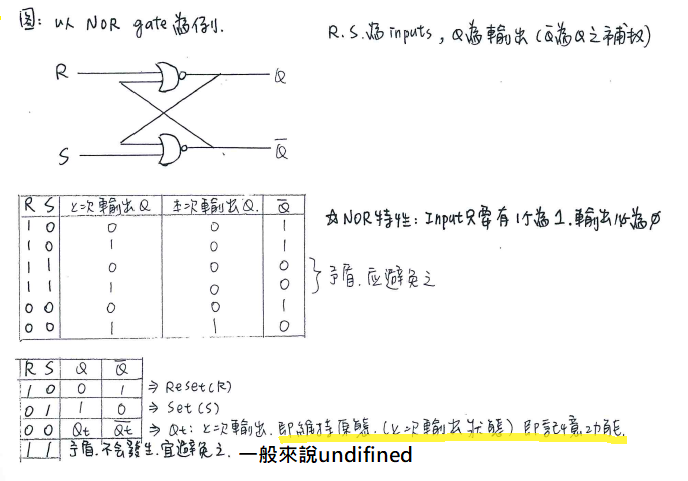


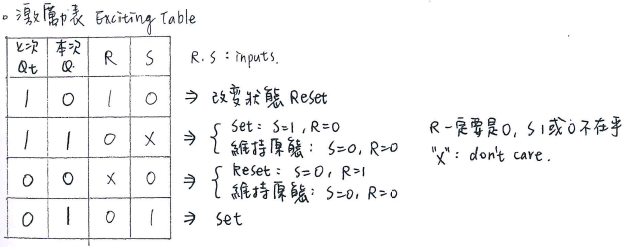




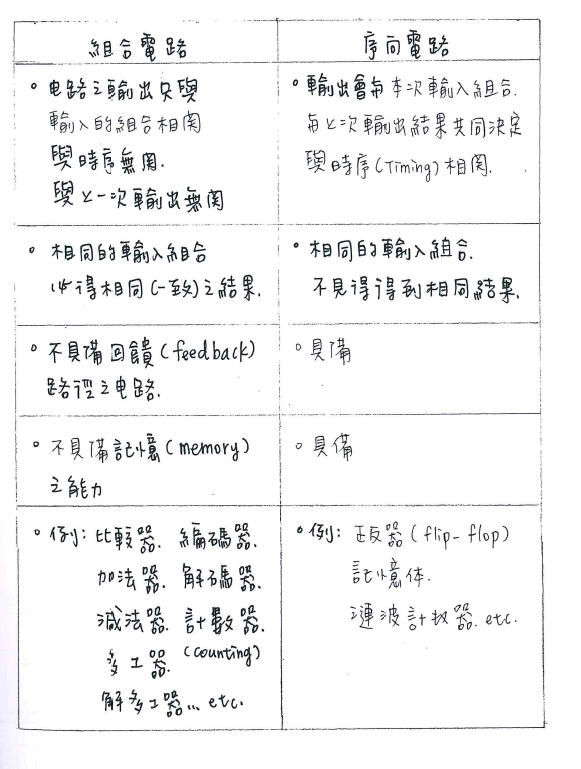


* + 序向電路(Sequential Circuit)
    - 正反器(Flip-Flop)

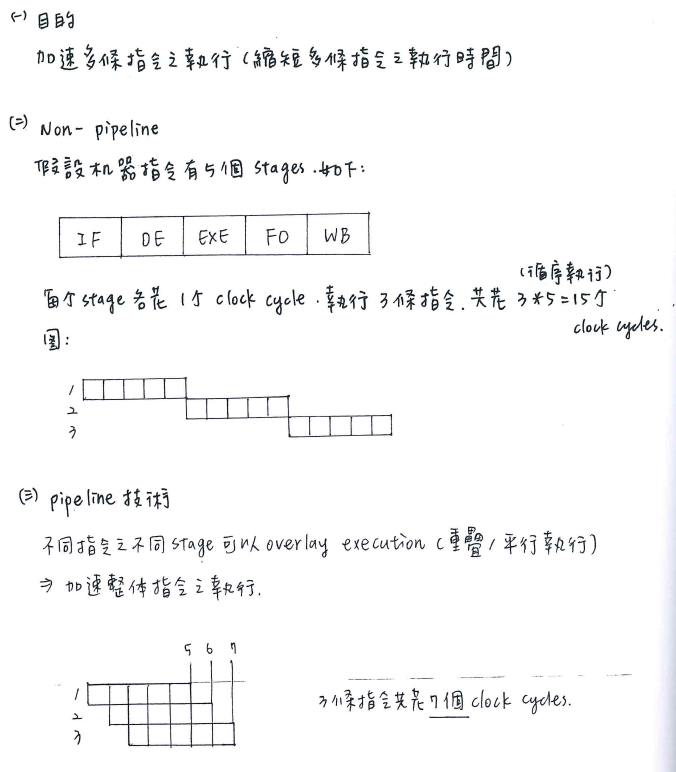


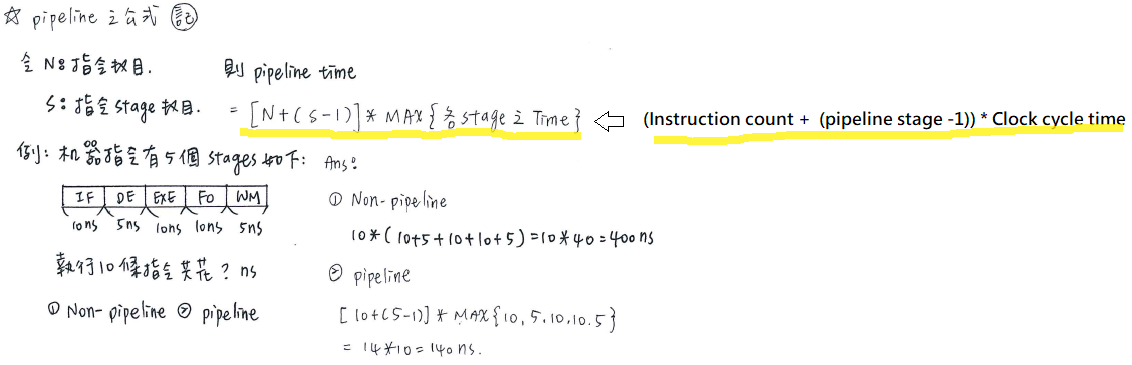


* + 比較



1. Pineline(管線式)
   * 公式
     + (Instruction count + (pipeline stage -1)) \* Clock cycle time
     + 執行到最後一條指令時，還需等(stage – 1)個cycle，作後一個指令才會完全做完





1. 命題演算

